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**Bartling et al.**

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(54) **POSITIVE EDGE PRESET RESET FLIP-FLOP WITH DUAL-PORT SLAVE LATCH**

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This patent is subject to a terminal disclaimer.

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**Related U.S. Application Data**

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(51) **Int. Cl.**
*H03K 3/289* (2006.01)
*H03K 3/3562* (2006.01)
*G11C 11/419* (2006.01)

(52) **U.S. Cl.**
CPC .......... ***H03K 3/35625*** (2013.01); ***G11C 11/419*** (2013.01)

(58) **Field of Classification Search**
USPC ......... 327/199, 202, 203, 208, 210–212, 214, 327/215, 218, 219
See application file for complete search history.

(56) **References Cited**

U.S. PATENT DOCUMENTS

| | | | | |
|---|---|---|---|---|
| 6,938,225 | B2 | 8/2005 | Kundu | |
| 7,908,500 | B2 * | 3/2011 | Westwick et al. | 713/323 |
| 8,803,582 | B1 * | 8/2014 | Bartling et al. | 327/202 |
| 8,829,963 | B1 * | 9/2014 | Bartling et al. | 327/202 |
| 2007/0001732 | A1 | 1/2007 | Branch et al. | |
| 2009/0058484 | A1 * | 3/2009 | Rao et al. | 327/202 |

FOREIGN PATENT DOCUMENTS

WO 03100830 A2 12/2003

* cited by examiner

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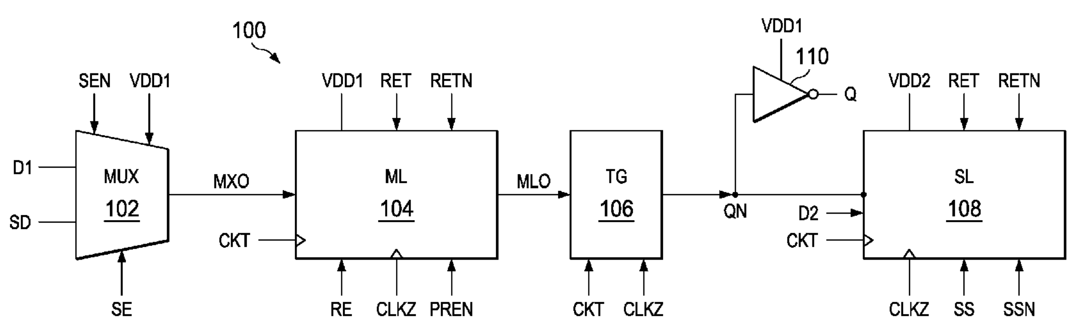
(57) **ABSTRACT**

In an embodiment of the invention, a flip-flop circuit contains a 2-input multiplexer, a master latch, a transfer gate and a slave latch. The scan enable control signals SE and SEN of the multiplexer determine whether data or scan data is input to the master latch. Clock signals CKT and CLKZ and retention control signals RET and RETN determine when the master latch is latched. The slave latch is configured to receive the output of the master latch, a second data bit D**2**, the clock signals CKT and CLN, the retain control signals RET and RETN, the slave control signals SS and SSN. The signals CKT, CLKZ, RET, RETN, SS, SSN and PREN determine whether the output of the master latch or the second data bit D**2** is latched in the slave latch. Control signals RET and RETN determine when data is stored in the slave latch during retention mode.

**10 Claims, 7 Drawing Sheets**



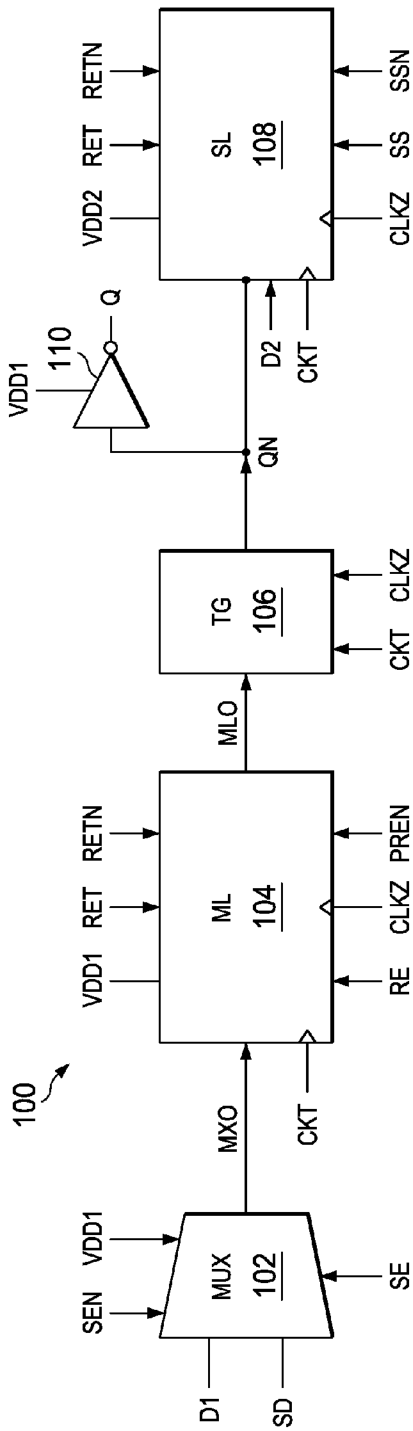

100
D1
SD
SEN
VDD1
MUX
102
SE
MXO
CKT
VDD1
RET
RETN
ML
104
RE
CLKZ
PREN
MLO
TG
106
CKT
CLKZ
QN
VDD1
110
Q
D2
CKT
VDD2
RET
RETN
SL
108
CLKZ
SS
SSN

FIG. 1

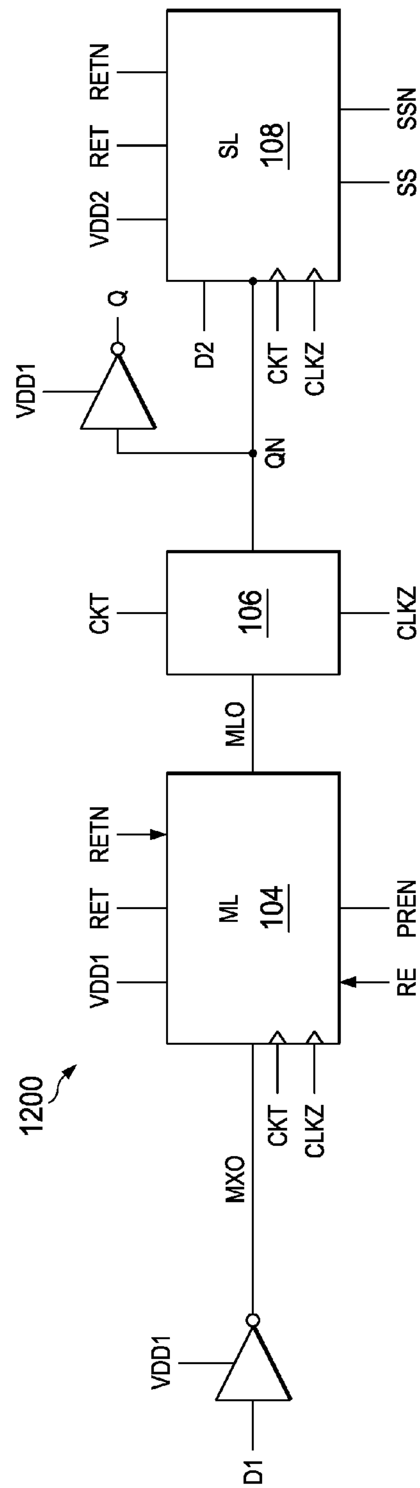

1200
D1
VDD1
MXO
CKT
CLKZ
VDD1
RET
RETN
ML
104
RE
PREN
MLO
CKT
106
CLKZ
QN
VDD1
Q
D2
CKT
CLKZ
VDD2
RET
RETN
SL
108
SS
SSN

FIG. 12

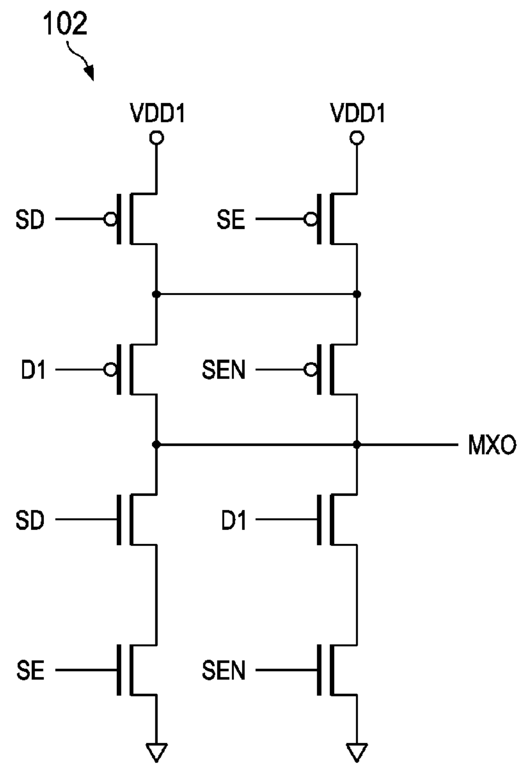



FIG. 2
(PRIOR ART)

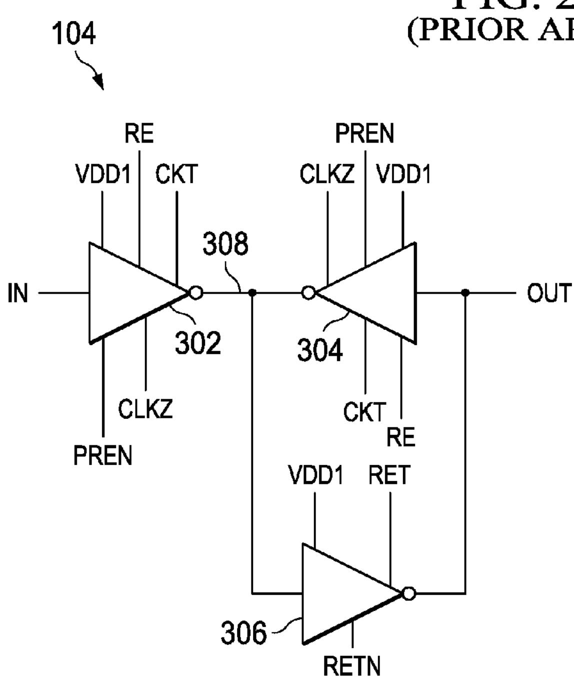



FIG. 3
(PRIOR ART)

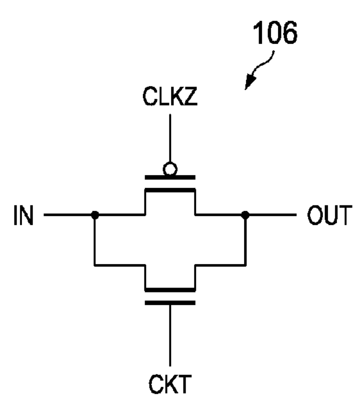



FIG. 4
(PRIOR ART)

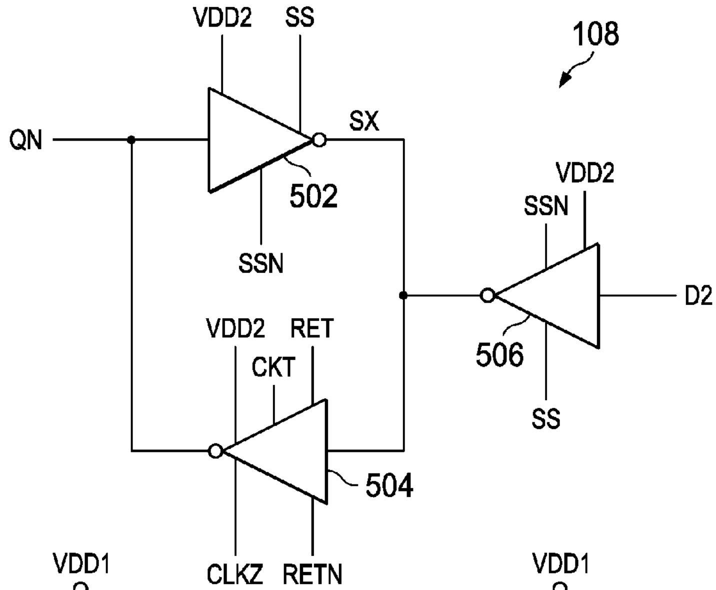
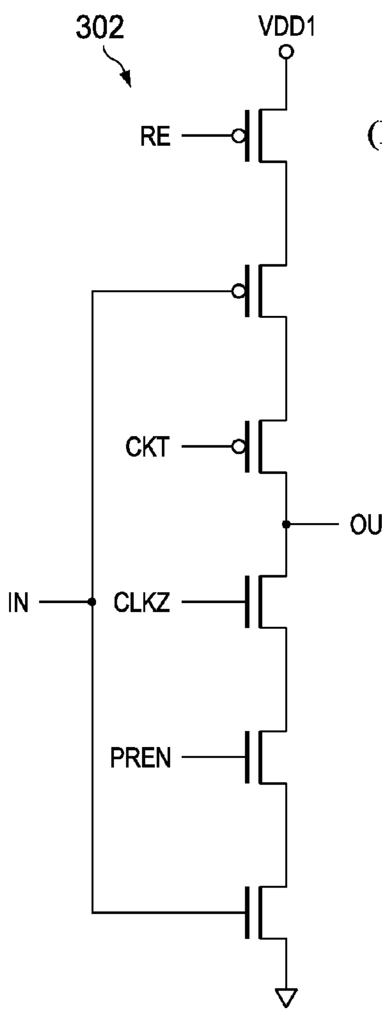



FIG. 5
(PRIOR ART)



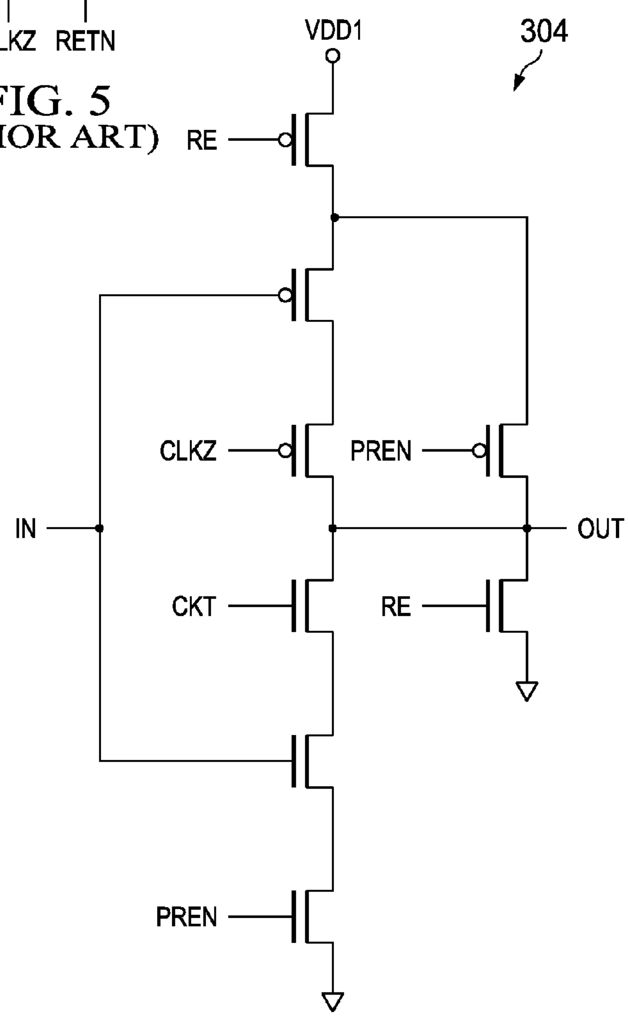




FIG. 6 (PRIOR ART)

FIG. 7 (PRIOR ART)

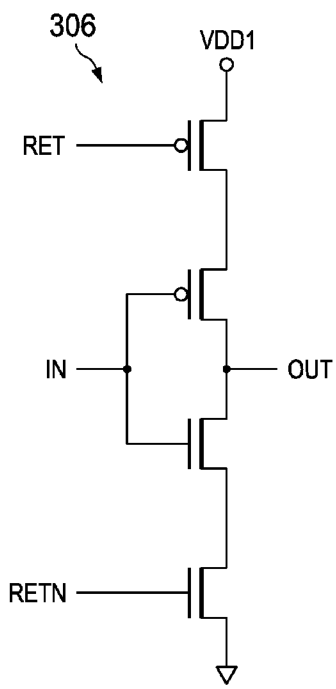



FIG. 8
(PRIOR ART)

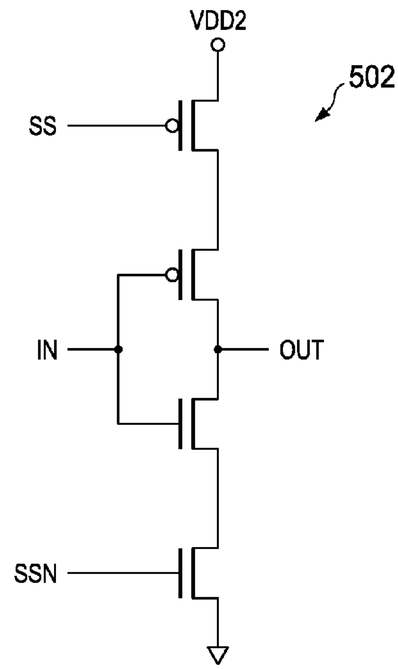



FIG. 9
(PRIOR ART)

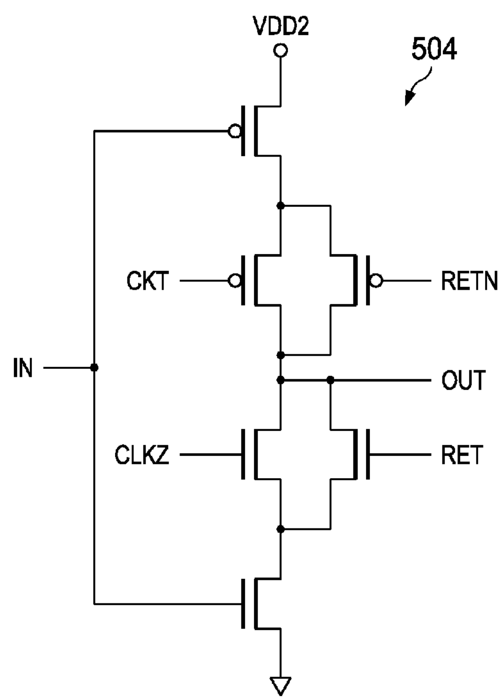



FIG. 10
(PRIOR ART)

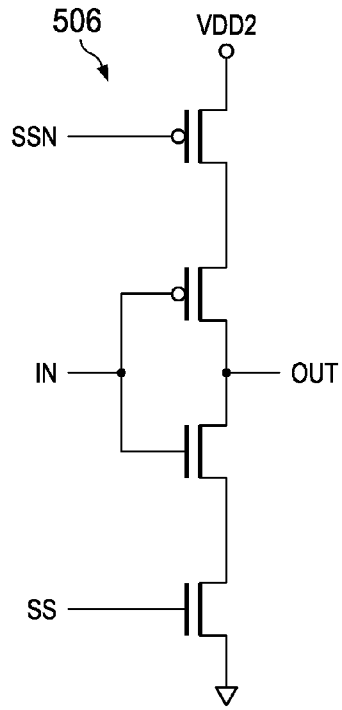



FIG. 11
(PRIOR ART)

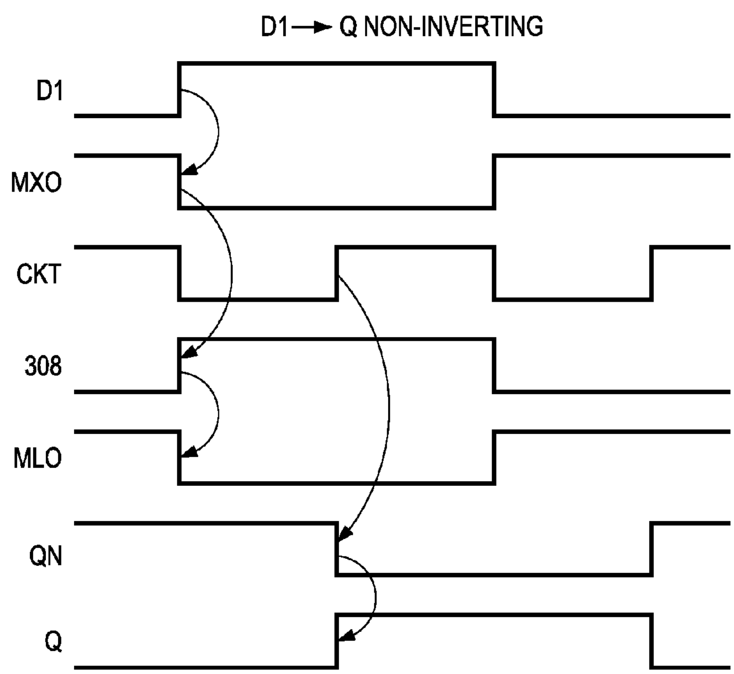



FIG. 13

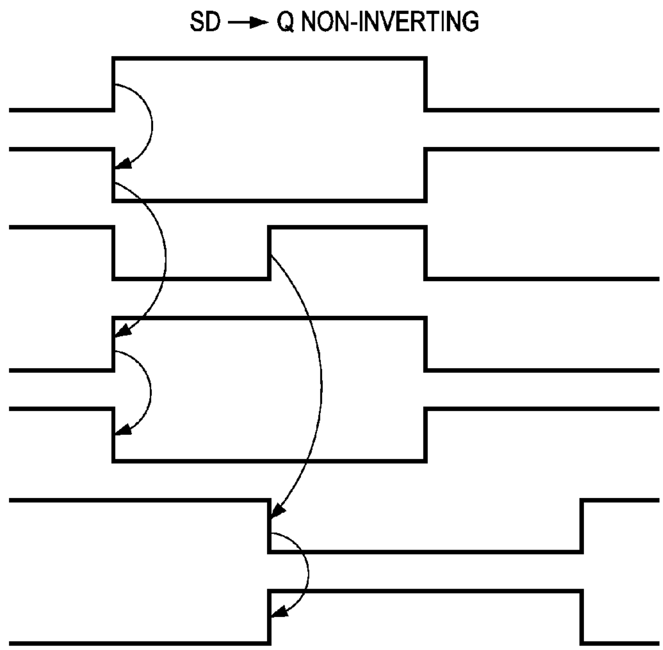

SD → Q NON-INVERTING
SD
MXO
CKT
308
MLO
QN
Q

FIG. 14

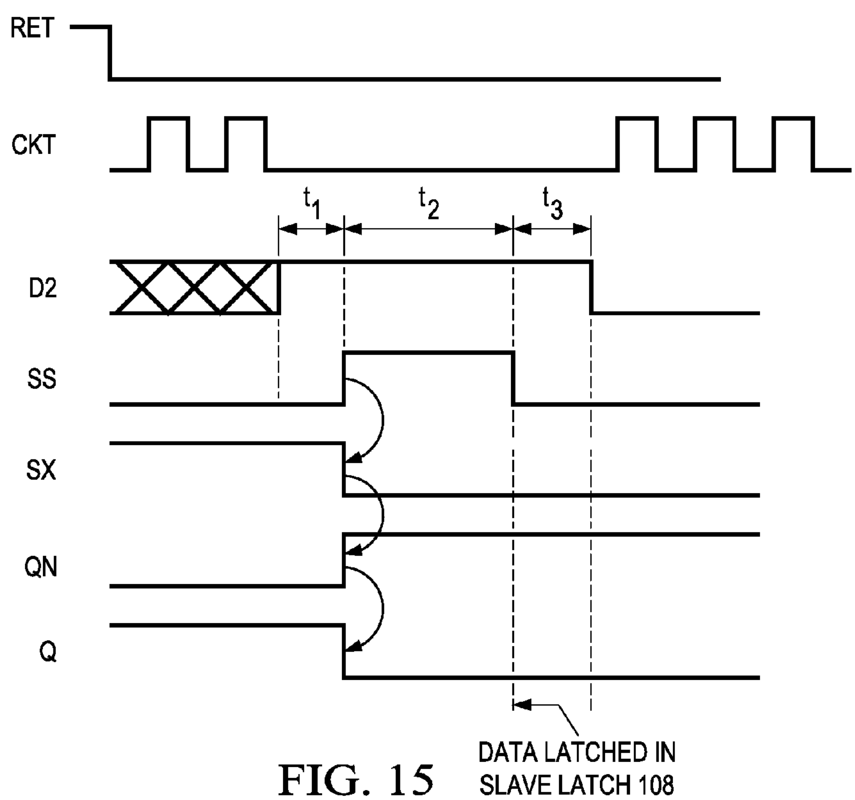

RET
CKT
$t_1$
$t_2$
$t_3$
D2
SS
SX
QN
Q
DATA LATCHED IN SLAVE LATCH 108

FIG. 15

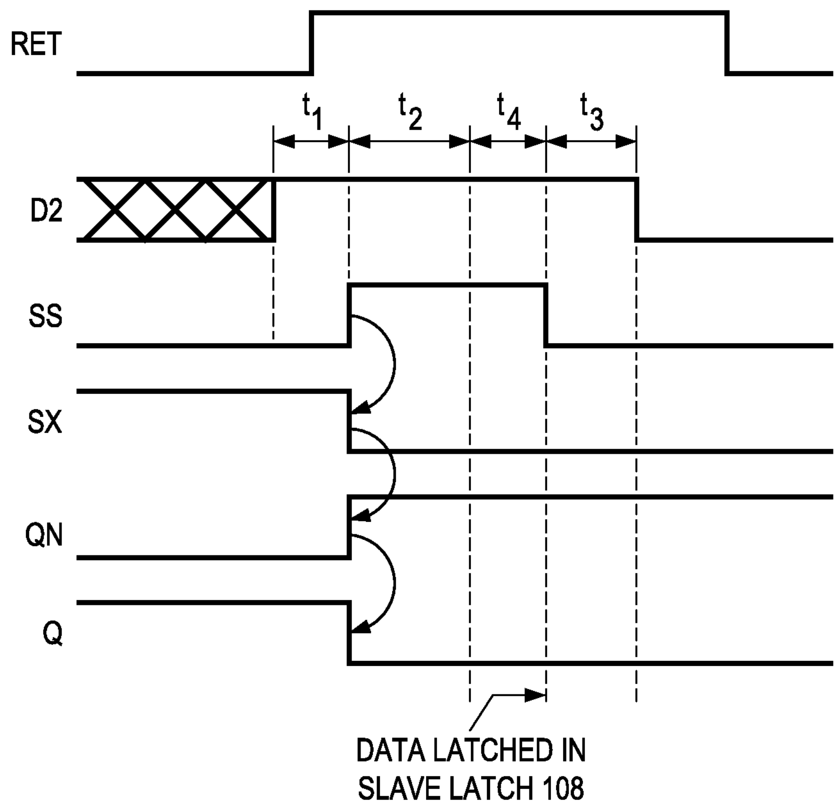



FIG. 16

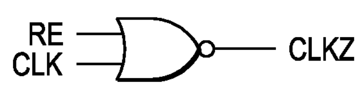



FIG. 17A

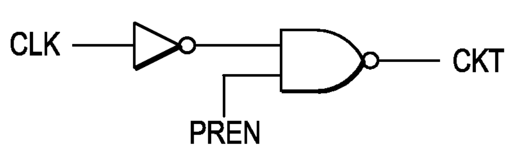



FIG. 17B

# POSITIVE EDGE PRESET RESET FLIP-FLOP WITH DUAL-PORT SLAVE LATCH

This application claims priority from Provisional Application No. 61/766,418, filed Feb. 19, 2013.

## BACKGROUND

Several trends presently exist in the semiconductor and electronics industry. Devices are continually being made smaller, faster and requiring less power. One reason for these trends is that more personal devices are being fabricated that are relatively small and portable, thereby relying on a battery as their primary supply. For example, cellular phones, personal computing devices, and personal sound systems are devices that are in great demand in the consumer market. It is also important that data on these devices be retained even when no power is supplied to the electronic device. Non-volatile memory circuits and non-volatile logic circuits are often used to meet these requirements.

Non-volatile logic implementation often requires updating sequential elements, such as flip-flops, from a source external to the sequential element, such as a non-volatile memory. When non-volatile logic circuits are implemented to allow the updating of sequential elements, it is desired that the implementation of the non-volatile logic circuit does not significantly slow the operation of a sequential element.

## BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1** is a block diagram of a scan-able positive edge reset preset flip-flop with a dual-port slave latch according to an embodiment of the invention.

FIG. **2** is a schematic diagram of a 2-to-1 multiplexer according to an embodiment of the invention. (Prior Art)

FIG. **3** is a schematic diagram of a master latch according to an embodiment of the invention. (Prior Art)

FIG. **4** is a schematic diagram of transfer gate. (Prior Art)

FIG. **5** is a schematic diagram of a dual-port slave latch according to an embodiment of the invention.

FIG. **6** is a schematic diagram of a clocked inverter according to an embodiment of the invention. (Prior Art)

FIG. **7** is a schematic diagram of a clocked inverter according to an embodiment of the invention. (Prior Art)

FIG. **8** is a schematic diagram of a tri-state inverter according to an embodiment of the invention. (Prior Art)

FIG. **9** is a schematic diagram of a tri-state inverter according to an embodiment of the invention. (Prior Art)

FIG. **10** is a schematic diagram of a clocked inverter according to an embodiment of the invention. (Prior Art)

FIG. **11** is a schematic diagram of a tri-state inverter according to an embodiment of the invention. (Prior Art)

FIG. **12** is a block diagram of a positive edge preset, reset flip-flop with a dual-port slave latch according to an embodiment of the invention.

FIG. **13** is a timing diagram showing data bit D**1**, MXO, clock signal CKT, MLO, QN and the output of the flip-flop Q according to an embodiment of the invention.

FIG. **14** is a timing diagram showing scan data bit SD, MXO, clock signal CKT, MLO, QN and the output of the flip-flop Q according to an embodiment of the invention.

FIG. **15** is a timing diagram showing signals D**2**, SS, SX, QN, and Q according to an embodiment of the invention.

FIG. **16** is a timing diagram showing signals RET, D**2**, SS, SX, QN, and Q according to an embodiment of the invention.



FIG. **17**A is a schematic diagram of an internal clock generating circuit according to an embodiment of the invention.

FIG. **17**B is a schematic diagram of an internal clock generating circuit according to an embodiment of the invention.

## DETAILED DESCRIPTION

In an embodiment of the invention, a flip-flop circuit contains a 2-input multiplexer, a master latch, a transfer gate and a slave latch. The multiplexer is configured to receive a first data bit D**1**, a scan data bit SD, a scan enable control signal SE and a binary logical compliment signal SEN of the scan enable control signal SE. The scan enable control signals SE and SEN determine when the data output MXO of the multiplexer is the compliment of data bit D**1** or scan data bit SD. The master latch is configured to receive the data output MXO from the multiplexer, a clock signal CKT, a binary logical compliment signal CLKZ of the clock signal CKT, a retain control signal RET, the binary logical compliment signal RETN of the retain control signal RET, a preset signal PREN and a reset signal RE. The signals CKT, CLKZ, RET, RETN, PREN and RE determine when the binary logical value of the data output MXO from the multiplexer is presented on the output MLO of the latch and when the MLO of the master latch is latched in the master latch or when MLO is tri-stated or is driven low.

A transfer gate transfers data from the output MLO of the master latch to the slave latch when the clock signal CKT transitions from a low logical value to a logical high value, when PREN transitions from an inactive state (logical 1) to an active state (logical 0) and when RE transitions from an inactive state (logical 0) to an active state (logical 1). The slave latch is configured to receive the output of the transfer gate, a second data bit D**2**, the clock signal CKT, the binary logical compliment signal CLKZ of the clock signal CKT, the retain control signal RET, the binary logical compliment signal RETN of the retain control signal RET, a slave control signal SS and the binary logical compliment signal SSN of the slave control signal SS. The signals CKT, CLKZ, RET, RETN, SS and SSN determine whether the binary logical value of the output of transfer gate or the second data bit (D**2**) is latched in the slave latch.

Non-volatile logic implementations often require updating sequential elements (e.g. flip-flops) from an external source (e.g. non-volatile memory). In an embodiment of the invention, the slave latch includes a second data input (port). The second data input is used to insert data from an external source. A tri-state inverter is added to the slave latch to accommodate the second data input. This will be explained in more detail later in the specification. When external data needs to be inserted into the slave latch, the tri-state inverter is enabled. During this time, the latch feedback is disabled by causing a forward inverter to be tri-stated with the opposite control signal as the former tri-state inverter.

The circuitry used to add the second input to the slave latch is not part of the critical timing path of the flip-flop. As a result, change to the regular performance of the flip-flop is negligible.

FIG. **1** is a block diagram of a scan-able positive edge preset reset flip-flop **100** with a dual-port slave latch **108** according to an embodiment of the invention. In a functional (i.e. normal) mode of operation, the scan enable signal SE is driven to a logical low level and the binary compliment signal SEN of SE is held at a logical high level. Because the flip-flop **100** is being operated in the functional mode, the retention mode signal RET is held at a logical low level, the binary compliment signal RETN of signal RET is held at a logical high level, the slave control signal SS is held at a logical low level, the binary compliment signal SSN of the slave control signal SS is held a logical high level, PREN is held at a logical high level and RE is held at a logical low level. Power is needed for functional mode operation so power supply VDD**1** and power supply VDD**2** are applied to the flip-flop **100**.

FIG. **13** is a timing diagram showing data bit D**1**, clock signal CKT and the output of the flip-flop Q during the functional mode of operation. Because the scan signal SE is low, the binary logical compliment of D**1** is passed to the output MXO of the multiplexer. FIG. **2** illustrates an embodiment of a 2-to-1 multiplexer **102**. The signal output MXO is then presented to the input IN of the master latch **104**. FIG. **3** is a schematic diagram of a master latch **104** according to an embodiment of the invention. The master latch **104** includes a first clocked inverter **302** (see FIG. **6** for an embodiment of the first clocked inverter **302**), a second clocked inverter **304** (see FIG. **7** for an embodiment of the second clocked inverter **304**) and a tri-state inverter **306** (see FIG. **8** for an embodiment of the tri-state inverter **306**) with tri-state controls RET and RETN. The clock signals CKT and CLKZ are generated from external clock CLK, RE and PREN (see FIGS. **17**A and **17**B).

When the clock signal CKT transitions from a high to a low logical level, the logical compliment of the data on the input IN of the master latch **104** is presented on node **308** of the master latch **104**. Because the flop-flop **100** is operating in the functional mode, the tri-state inverter **306** is active and drives the output MLO of the master latch **104** to the same logical value as the input MXO of the master latch **104**. When the clock signal CKT transitions from the low logical level to a high logical level (i.e. positive edge of CKT), the logical level on node **308** is latched and the logical level on the output MLO of the master latch **104** is transferred by the transfer gate **106** to QN. Inverter **110** passes the complement of the output MLO of the master latch to the output Q. In this embodiment of the invention, the overall signal path from the input D**1** of the multiplexor **102** to the Q output of inverter **110** in the slave latch **108** is non-inverting. However, in other embodiments, the overall signal path can be inverting.

FIG. **4** is a schematic diagram of an embodiment of a transfer gate.

FIG. **5** is a schematic diagram of a dual-port slave latch **108** according to an embodiment of the invention. The slave latch **108** includes a first tri-state inverter **502** (see FIG. **9** for an embodiment of the first tri-state inverter **502**) with tri-state controls SS and SSN, a clocked inverter **504** (see FIG. **10** for an embodiment of the clocked inverter **504**) with controls RET and RETN and a second tri-state inverter **506** (see FIG. **11** for an embodiment of the second tri-state inverter **506**) with tri-state controls SS and SSN.

Because the flop-flop **100** is operating in the functional mode, the tri-state inverter **502** is active and drives node SX of the slave latch **108** to the complimentary logical value as the QN of the slave latch **108**. When the clock signal CKT transitions from a high logical level to a low logical level, the logical level on the QN is latched by the clocked inverter **504**. In this embodiment of the invention, an inverter **110** is used to buffer the QN of the slave latch **108**. However, non-inverting buffers may be used as well. The tri-state inverter **506** is tri-stated in this mode because SS is a logical low level and SSN is a logical high level. As a result, D**2** is not transferred to node SX.

However, during another functional mode of operation, data D**2** may be written directly to the slave latch **108** (See FIG. **15**). During this functional mode, the clock signal CKT is held at a low logical level and CLKZ is held at a high logical level with control signal SS held at a logical high level and control signal SSN held at logical low level. All other inputs to the slave **108** are don't-cares.

When control signal SS is held at a logical high level and control signal SSN is held at logical low level, tri-state inverter **506** is able to drive the complimentary value of D**2** onto node SX of the slave latch **108**. Because CKT and RET are held at logical low levels and CLKZ and RETN are held at logical high levels, the clocked inverter **504** is active and drives node QN to the logical value of D**2**. The inverter **110** then inverts the logical value on node QN to its compliment. In this example, the compliment of D**2** is presented on node Q. Data signal D**2** must be held for the period t**3** to insure that the correct value of D**2** is latched. Also, control signal SS must remain at logical high value for time t**2** to insure that the correct value D**2** is latched.

When control signal SS is driven from a logical high level to a logical low level and SSN is driven from a logical low level to a logical high level, the tri-state inverter **506** is tri-stated and tri-state inverter **502** becomes active latching the logical value on node QN of the slave latch **108**.

In a scan (i.e. test) mode of operation, the scan enable signal SE is driven to a high logical level and the binary compliment signal SEN of SE is held a logical low level. Because the flip-flop **100** is being operated in the scan mode, the retention mode signal RET is held at a logical low level, the binary compliment signal RETN of signal RET is held at a logical high level, the slave control signal SS is held at a logical low level, the binary compliment signal SSN of the slave control signal is held at a logical high level and PREN is held at a logical high level. Power is needed for functional scan operation so power supply VDD**1** and power supply VDD**2** are applied to the flip-flop **100**.

FIG. **14** is a timing diagram showing scan data bit SD, clock signal CKT and the output Q of the flip-flop **100** during a scan mode of operation. The scan data bit SD is received at an input of the 2-to-1 multiplexer **102**. Because the scan signal SE is high, the binary logical compliment of SD is passed to the output MXO of the multiplexer. When in the scan mode, the master latch **104**, the transfer gate **106** and the slave latch **108** latch operate in the same manner as they did during the functional mode as previously described.

The flip-flop **100** can also be operated to retain data (RET mode) in the slave latch **108** (power supply VDD**2** is active) while the 2-to-1 multiplexer **102**, the master slave **104** and the inverter **110** are powered off (i.e. power supply VDD**1** is inactivated). In RET mode of operation, the value of the SE, SEN and PREN don't matter. Because the flip-flop **100** is being operated in the RET mode, the retention mode signal RET is held at a logical high level and the binary compliment signal RETN of signal RET is held at a logical low level. In this embodiment, the slave control signal SS is held at a logical low level, and the binary compliment signal SSN of the slave control signal is held at a logical high level. The value of the clock signals CKT and CLKZ don't matter. As stated earlier, power is only applied to the slave latch **108** by power supply VDD**2**.

Because power is not supplied to the 2-to-1 multiplexer **102** and the master latch **104**, the data presented to the input IN of the transfer gate **106** is guaranteed not to have a path to VDD or ground (VSS) via the RET and RETN functionality embodied in the tri-state inverter **306** in the master latch **104**. In this manner, the data being retained in the slave latch **108** will not be inadvertently corrupted by the indeterminate value of the input to the tri-state inverter **308** (the input is indeterminate as the supply VDD**1** is inactive or floating).

Because the flop-flop **100** is operating in the retention mode, the tri-state inverter **502** is active and drives node SX of the slave latch **108** to the complimentary logical value of the value stored on QN of the slave latch **108**. Because RET is a logical high value and RETN is a logical low value, the clocked inverter **504** latches the logical value on QN. The tri-state inverter **506** is tri-stated in this mode because SS is a logical low level and SSN is a logical high level. As a result, the logical value on D**2** is not transferred to node SX.

However, during another retention mode of operation, data D**2** may be written directly to the slave latch **108**. During this retention mode, the slave control signal SS is driven to a logical high level following RET being driven to a logical high value (see FIG. **16**). The clock signals CKT and CLKZ and the scan enable signals SE and SEN are don't cares in this mode of operation in this embodiment. Before time t**1**, D**2** does not have to be driven to a logical level (i.e. D**2** may be a logical one, a logical zero, floating or tri-stated). D**2** must be driven to a logical one or a logical zero some time t**1** before the control signal SS transitions from a logical zero to a logical one. D**2** must be stable for time t**4** before the control signal SS transitions from a logical one to a logical zero and remain stable for time t**3** afterwards in order to ensure D**2** will be correctly latched.

Because the slave control signal SS is driven to a logical high level following RET being driving to a logical high value, the tri-state inverter **502** is tri-stated and does not drive node SX of the slave latch **108**. Because the slave control signal SS is driven to a logical high and slave control signal SSN is driven to a logical low value, the tri-state inverter **506** is active and drives node SX to the complimentary value presented on D**2**. Because RET is a logical high value and RETN is a logical low value, the clocked inverter **504** is active and drives node QN. When the slave control signal SS returns to a logic low level and SSN returns to a logic high level, the value stored on node QN is latched between tri-state inverter **502** and clocked inverter **504** while tri-state inverter **506** is tri-stated. Data signal D**2** must be held for the period t**3** to insure that the correct value of D**2** is latched. Also, control signal SS must remain at logical high value for time (t**2**+t**4**) to insure that the correct value D**2** is latched. Under this condition, the data written from D**2** remains latched in the slave latch **108** during retention mode.

FIG. **12** is a block diagram of a positive edge reset, preset flip-flop **1200** with a dual-port slave latch **108** according to an embodiment of the invention. In this embodiment, the positive edge flip-flop is not scan-able for test purposes. The rest of the flip-flop functions as previously described for FIG. **1**.

When an embodiment of the invention is asynchronously preset during functional mode (i.e. the preset signal can be issued at any time irrespective of the logical value of the clock signal and the master and slave stages of the flip-flop will be preset), the master latch **104** shown in FIGS. **1** and **12** may be initialized to a logical zero on its output MLO by driving PREN to a logical zero. As result, the output of clocked inverter **302** is tri-stated. Because PREN is driven to a logical zero and the output of clocked inverter **302** is prevented from driving its output to a logic zero, node **308** of the master latch **104** is driven to a logical one. As a result, the output of inverter **306** is driven to a logical zero. Because PREN is driven to a logical zero, the clock generator circuit shown in FIGS. **17**A and **17**B drives signal CKT to a logical one. Because CKT is a logical one, the NFET in pass gate **106** is activated, providing a path for a logical zero to propagate from the output of inverter **306** onto slave latch node QN and via slave latch inverter **110** to the output Q to produce a logic one at the flip-flop output Q.



When an embodiment of the invention is asynchronously reset during functional mode (i.e. the reset signal can be issued at any time irrespective of the logical value of the clock signal and the master and slave stages of the flip-flop will be reset), the master latch **104** shown in FIGS. **1** and **12** may be initialized to a logical one on its output MLO by driving RE to a logical one. As result, the output of clocked inverter **302** is tri-stated. Because RE is driven to a logical one and the output of clocked inverter **302** is prevented from driving its output to a logic one, node **308** of the master latch **104** is driven to a logical zero. As a result, the output of inverter **306** is driven to a logical one. Because RE is driven to a logical one, the clock generator circuit shown in FIGS. **17**A and **17**B drives signal CKZ to a logical zero. Because CKZ is a logical zero, the PFET in pass gate **106** is activated, providing a path for a logical zero to propagate from the output of inverter **306** onto slave latch node QN and via slave latch inverter **110** to the output Q to produce a logic zero at the flip-flop output Q.

Inverters internal to the flip-flops **100** and **1200** may be used in an embodiment of the invention to invert signals SE, RET and SS.

The foregoing description has been presented for purposes of illustration and description. It is not intended to be exhaustive or to limit the invention to the precise form disclosed, and other modifications and variations may be possible in light of the above teachings. The embodiments were chosen and described in order to best explain the applicable principles and their practical application to thereby enable others skilled in the art to best utilize various embodiments and various modifications as are suited to the particular use contemplated. It is intended that the appended claims be construed to include other alternative embodiments except insofar as limited by the prior art.

What is claimed is:

**1**. A flip-flop circuit comprising:

a multiplexer configured to receive a first data bit (D**1**), a scan data bit (SD), a scan enable control signal (SE) and a binary logical compliment signal (SEN) of the scan enable control signal (SE), wherein the scan enable control signals (SE) and (SEN) determine whether a data output (MXO) of the multiplexer is the binary compliment of data bit (D**1**) or the binary compliment of scan data bit (SD);

a master latch configured to receive the data output (MXO) of the multiplexer, a first clock signal (CKT), a second clock signal (CLKZ), a retain control signal (RET), a binary logical compliment signal (RETN) of the retain control signal (RET), a reset signal (RE) and a preset signal (PREN), wherein the signals (CKT), (CLKZ), (RET), (RETN), (RE) and (PREN) determine when the binary logical value of the data output (MXO) is presented on an output (MLO) of the master latch and when the output (MLO) of the master latch is latched in the mater latch;

a transfer gate wherein the transfer gate transfers data from the output (MLO) of the master latch to an output of the transfer gate when the first clock signal (CKT) transitions from a low logical value to a logical high value; wherein the transfer gate transfers data from the output (MLO) of the master latch to the output of the transfer gate when signal PREN transitions from an logical one to a logical zero; wherein the transfer gate transfers data from the output (MLO) of the master latch to the output of the transfer gate when the signal RE transitions from an logical zero to a logical one;

a slave latch configured to receive the output of the transfer gate, a second data bit (D**2**), the first clock signal (CKT), the second clock signal (CLKZ), the retain control signal (RET), the binary logical compliment signal (RETN) of the retain control signal (RET), a slave control signal (SS) and a binary logical compliment signal (SSN) of the slave control signal (SS) wherein the signals (CKT), (CLKZ), (RET), (RETN), (SS) and (SSN) determine whether the output of the transfer gate or the second data bit (D**2**) is latched in the slave latch; wherein the output of the transfer gate is (QN).

**2**. The flip-flop circuit of claim **1** wherein the multiplexer and the master latch receive power from a first power supply (VDD**1**); wherein the slave latch receives power form a second power supply (VDD**2**).

**3**. The flip-flop of claim **2** wherein the first power supply (VDD**1**) is turned off and the second power supply (VDD**2**) is turned on during operation of a retention mode; wherein power is only supplied to the slave latch.

**4**. The flip-flop of claim **1** wherein the signals (SS), (SSN), (RET), (RETN), (RE) and (PREN) are controlled external to the flip-flop to prevent data contention between the output of the transfer gate and the second data bit (D**2**).

**5**. The flip-flop of claim **1** wherein the master latch comprises:

a first clocked inverter, the first clocked inverter having a data input, four control inputs and a data output wherein the data input is electrically connected to the data output (MXO), the first control input is electrically connected to (CKT), the second control input is connected to (CLKZ), the third control input is connected to (PREN) and the fourth control input is connected to (RE);

a tri-state inverter, the tri-state inverter having a data input, two control inputs and a data output wherein the data input is electrically connected to the data output of the first clocked inverter, the first control input is electrically connected to (RET) and the second control input is connected to (RETN);

a second clocked inverter, the second clocked inverter having a data input, four control inputs and a data output wherein the data input is electrically connected to the data output of the tri-state inverter, the first control input is electrically connected to (CKT), the second control input is connected to (CLKZ), the third control input is electrically connected to (PREN), the fourth control input is electrically connected to (RE) and the output of the second clocked inverter is electrically connected to the output of the first clocked inverter and to the input of the a tri-state inverter.

**6**. The flip-flop of claim **1** wherein the transfer gate comprises:

an NMOS transistor having a gate, drain and source wherein the gate of the NMOS transistor is electrically connected to (CKT);

a PMOS transistor having a gate, drain and source wherein the gate of the PMOS transistor is electrically connected to (CLKZ), the drains of the NMOS and PMOS transistors are electrically connected and the sources of the NMOS and PMOS transistors are electrically connected.

**7**. The flip-flop of claim **1** wherein the slave latch comprises:

a first tri-state inverter, the first tri-state inverter having a data input, two control inputs and a data output wherein the data input is electrically connected to the output of the transfer gate, the first control input is electrically connected to (SS), and the second control input is connected to (SSN);

a second tri-state inverter, the second tri-state inverter having a data input, two control inputs and a data output wherein the data input is electrically connected to the second data bit (D**2**), the first control input is electrically connected to (SS), and the second control input is connected to (SSN) and the outputs of the first and second tri-state inverter are electrically connected to each other;

a clocked inverter, the clocked inverter having a data input, four control inputs and a data output wherein the data input is electrically connected to the data output of the first and second tri-state inverters, a first control input is electrically connected to (CKT), a second control input is connected to (CLKZ), a third control input is electrically connected to (RET), a fourth control input is electrically connected to (RETN) and the output of the clocked inverter is electrically connected to the input of the first tri-state inverter.

**8**. The flip-flop circuit of claim **1**, further comprising a third inverter wherein the third inverter receives the retain control signal (RET) and the third inverter outputs the binary logical compliment signal (RETN) of the retain control signal (RET).

**9**. The flip-flop circuit of claim **1**, further comprising a fourth inverter wherein the fourth inverter receives the slave control signal (SS) and the fourth inverter outputs the binary logical compliment signal (SSN) of the slave control signal (SS).

**10**. The flip-flop circuit of claim **1**, further comprising a fifth inverter wherein the fifth inverter receives the scan enable control signal (SE) and the fifth inverter outputs the binary logical compliment signal (SEN) of the scan enable control signal (SS).

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